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# Design and Analysis of Different Adder Circuit Using Output Wired Cmos Logic Based Majority Gate

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***Abstract**: A new technique is introduced that combines the advantages of the output wired CMOS logic with the majority gate. The concept of majority gate is of utmost importance because it helps in reducing the delay produced in the circuits and output wired CMOS logic helps in reducing the transistor count. The adder circuits i.e. full adder, ripple carry adder and carry look ahead adder have been simulated for 130nm channel length. The results obtained show that this technique has an advantage of Delay reduction and reduced transistr count as compared to the conventional design. Simulation has been done using Tanner tool.*

***Keywords**: Adder, Complementary Metal Oxide Semiconductor (CMOS), full adder, Majority gate, ripple carry adder, carry look ahead adder*

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## I. Introduction

One of the basic fundamental arithmetic operation is addition. It is extensively used in application specific systems. The adder cell designed is based on majority gate and output wired CMOS logic. It helps in dealing with issues of power consumption, delay in output, transistor count and the area required for the design.

There are different implementation techniques for threshold gate based logic design[8,10,16,17]. Threshold gate can be implemented using capacitive threshold logic [6,7,9], output wired CMOS inverter [11,13], MOS-NDR based monostable bistable transistor logic.In this paper, we have designed one bit full adder CMOS circuit using output wired CMOS logic based majority gate. Further, the other adder circuits i.e. 4-bit ripple carry adder and 2 bit carry look ahead adder circuit has been designed using the same logic. A comparative study has been performed on the proposed designs and conventional designs and the simulation results show that the delay produced is less and the transistor count is also reduced.

Other sections in the paper include: Section II: Description of Concept of majority gate; Section III: Discussing concept of output wired CMOS logic; Section IV: Output wired CMOS logic based majority gate; Section V: Design of one bit full adder using output wired CMOS logic based majority gate; Section VI: Design of ripple carry adder using output wired CMOS logic based majority gate ;Section VII: Design of carry look ahead adder using output wired CMOS logic based majority gate; Section VIII: Comparison of proposed designs with conventional designs; Section IX: Conclusion.

## II. Concept Of Majority Gate

A majority gate [12,14] is a logical gate used in circuit complexity and other applications of Boolean circuits. In case of majority gate the output will be '1' if over half of the inputs are '1'otherwise it will be '0'. The majority gate usually consists of odd number of inputs represented as "w" as shown in fig. 1.

Mathematically, it is represented as :

$$\text{Majority } (p1, p2, \ldots . pn) = \left[\frac{1}{2} + \frac{\sum_{i=1}^{n} p_i - (\frac{1}{2})}{n}\right] \qquad (1)$$

In other words, the majority gate can be called a special case of threshold gate where the threshold value is equal to half of input plus one.

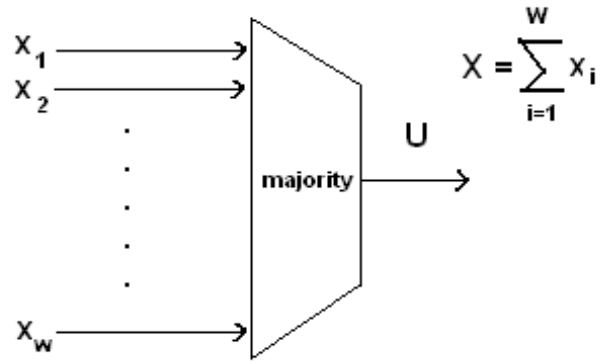


**Fig: 1** Majority gate function

Mathematically, $T = \frac{(w+1)}{2}$ (2)

As shown in the fig. 2, there are three inputs a, b and c and either of the two inputs are passed through the AND logic gate and the output obtained respectively are passed through the OR logic gate. Thus, the logic produced is:

$$q = ab + bc + ca \quad (2)$$

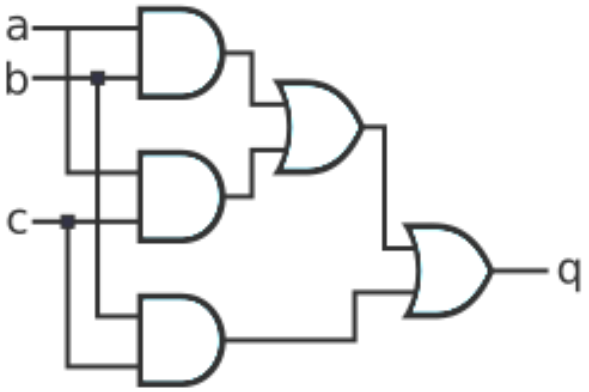


**Fig:2** 3 input majority gate

The circuit diagram for majority gate using CMOS is shown in fig 3. It is made up of two parts: a nonlinear voltage divider made up of output wired inverters on the left hand side and an inverting buffer which senses the majority transition and provides a positive output on the right. The output inverting buffer isolates the divider output node from external circuitry to reduce noise effect and driving from the next stage. It also reshapes the output waveforms.

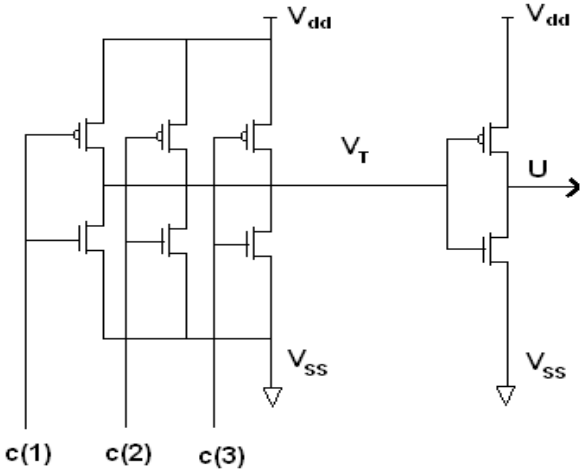


**Fig. 3** Circuit of three input majority gate

## III. Concept Of Output Wired Logic

A wired logic connection is a logic gate that implements Boolean algebra (logic) using only passive elements like resistors, capacitors. It also uses diode for the logic implementation when it's not behaving as an active device means when it has no negative differential resistance. A wired logic connection can create an AND or OR gate. Here, instead of AND and OR gate we have used CMOS as an element that helps to form the output wired CMOS logic.

## IV. Output Wired Cmos Logic Based Majority Gate

As shown in fig 4, each input $x_t$ drives one inverter, all inverter outputs shorted together to design a non linear voltage divider which drives output inverter whose purpose is to quantize the non binary signal at the ganged output node .

The PMOS and NMOS transistor widths of each inverter are designed depending on the weight (W) of each inputs and threshold is implemented by adjusting the threshold of the last inverter. The weight values other than 1 can be realized by changing the width of the PMOS transistor. Thus, the design process involves sizing only two inverters the basic input inverters and the output inverter.

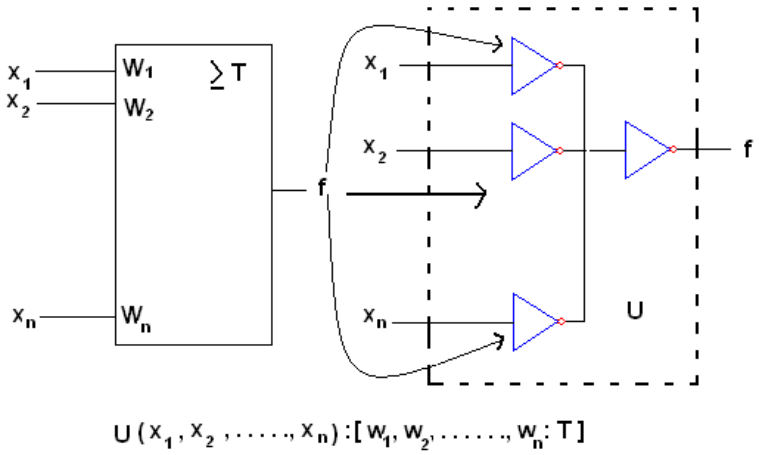


**Fig. 4** Nonstandard symbol of Threshold gate and threshold gate basic structure using output wired ganged CMOS

## V. Design Of One Bit Full Adder Using Output Wired Cmos Logic Based Majority Gate

One bit full adder [1,2,4] adds the three binary inputs to produce output where the two inputs are A and B and the third input the carry presented as Cin and the output produced are Sum and Carry (Cout).

Mathematically, sum and carry for full adder is represented as:

$$Sum = A \oplus B \oplus C_{in} \quad (3)$$

$$C_{out} = A.B + C_{in}(A \oplus B) \quad (4)$$

Generally, full adder circuit is presented as:

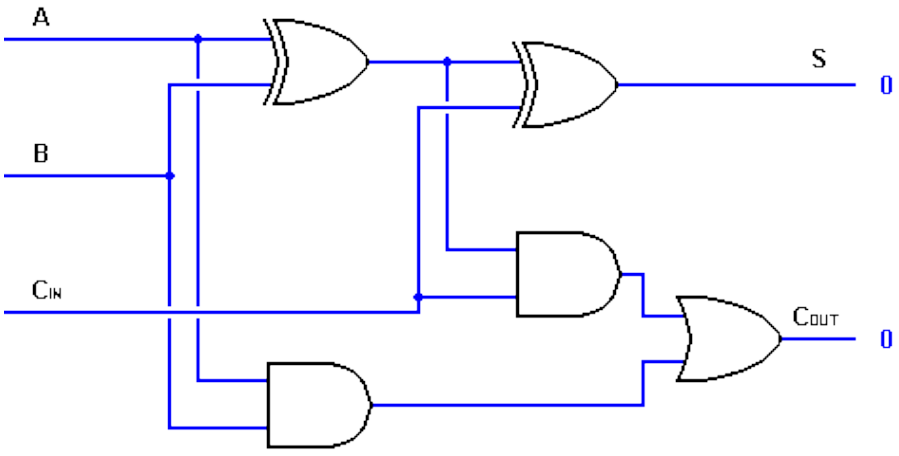


**Fig. 5** Full Adder Circuit

The threshold gate based implementation of full adder and the equivalent output wired ganged CMOS based one bit Full Adder circuit is shown in fig 6.

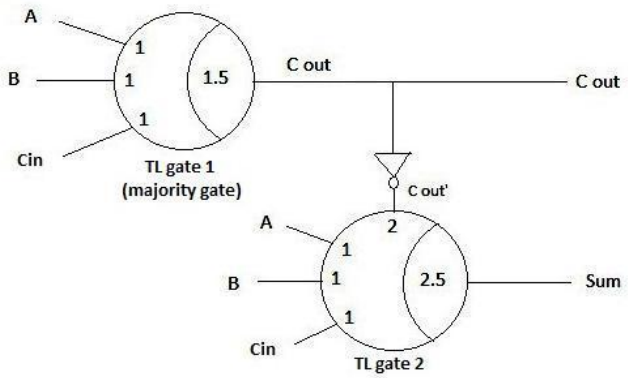


**Fig. 6** Threshold Logic gate based Full Adder Circuit.

Here two threshold gates are used TL gate1 and TL gate2.TL gate1 gives the carry output and it is a majority gate. This Majority gate is designed using four inverters. Three of them are ganged and from that ganged output, the fourth inverter is connected to get the carry output. Inputs of full adder (A, B, $C_{in}$) are applied to three inverters (INV1, INV2, INV3) which is shown in Fig. 7. The W/L ratio of all the PMOS and NMOS transistors are chosen such that the resistance of all the transistors are equal (R).So the equivalent circuit of ganged part may be considered as a voltage divider network.

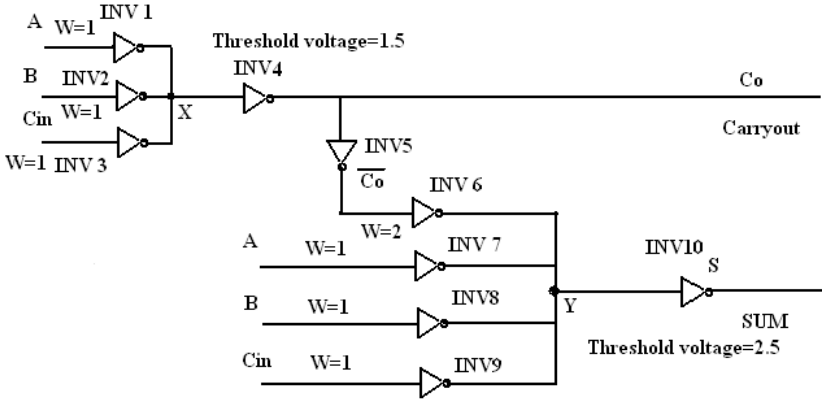


**Fig: 7** One bit Full Adder circuit using CMOS output wired logic based majority gate

The circuit has been designed using Tanner tool for 130 nm channel length. The below circuit consists of inverters and two outputs for carry and sum respectively. Threshold voltage for the last inverter after node X is calculated and it is found to be in between Vdd/3 to 2(Vdd)/3.Also, the threshold voltage for last inverter after node Y, i.e. Sum inverter is between (2/5)Vdd and (3/5)Vdd.

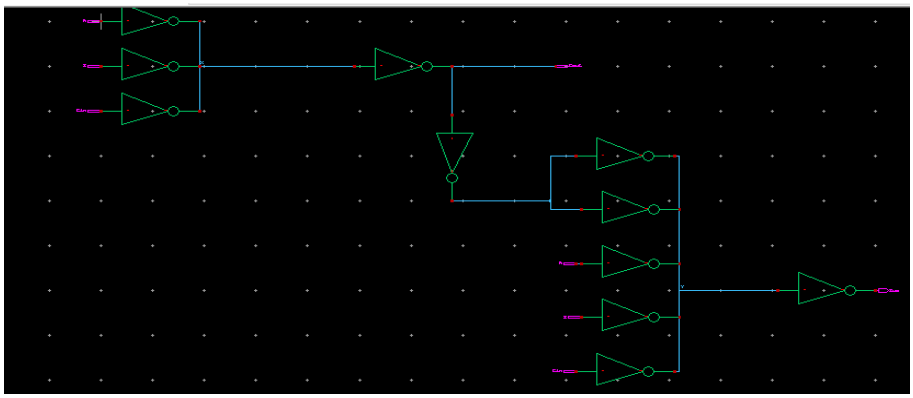

**Fig. 8** One bit full adder circuit using Tanner Tool

The following figure shows the output of one bit full adder for input streams of 01100110 , 01110111 and 10010111 as A,B and Cin respectively.

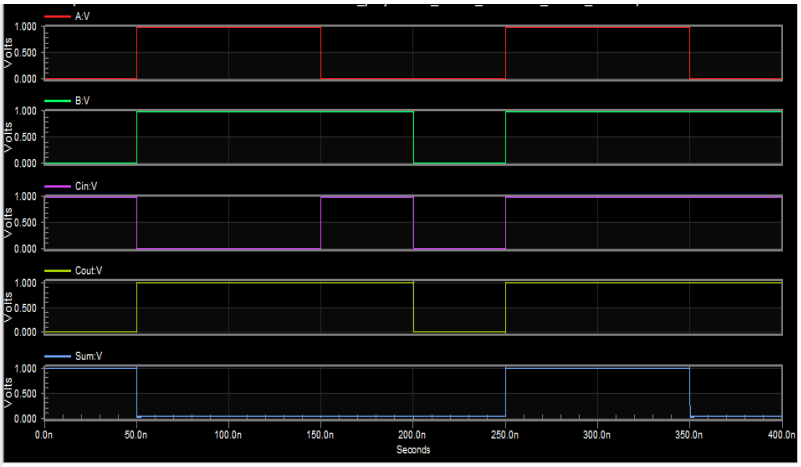


**Fig. 9** Output waveform for different set of inputs

Along with the outputs for sum and carry, the power consumed and delay is calculated for the above circuit and it is found that the power calculated is 4.311645e-004 watts and the delay produced is -199.7684n for carry whereas for the sum, the delay is -199.9362n in the best cases.

## VI. Design Of Ripple Carry Adder Using Output Wired Cmos Logic Based Majority Gate

Full adder [3,5]blocks can be cascaded in parallel to form N bit adders. A ripple carry [19,20] adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry[24,25] adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Here ripple carry adder is designed using the full adder block is shown in fig. 10

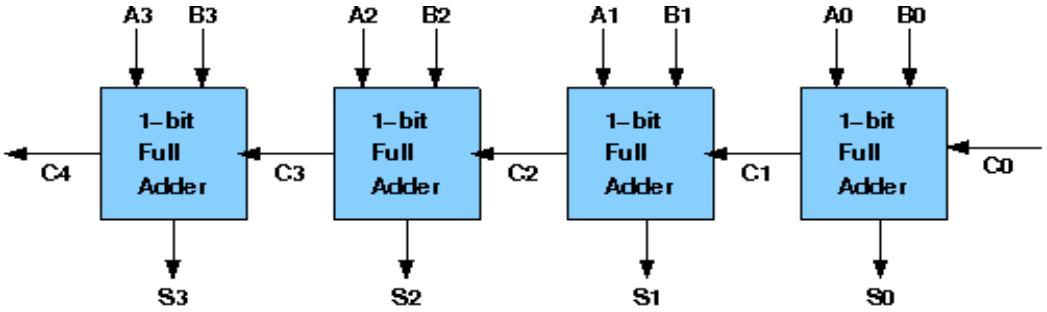


**Fig.10** Ripple Carry Adder block diagram

The circuit design using tanner tool is shown in fig.11 below. The circuit has been designed for 4 bit ripple carry adder. The carry output from one full adder is connected as input carry to the next full adder and the same is repeated for remaining blocks of full adder.

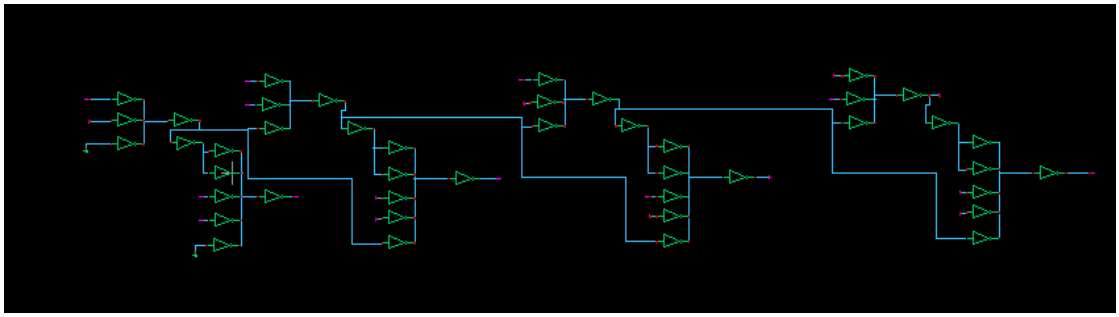

**Fig.11** Ripple Carry Adder using tanner tool

The following figure shows the output for four bit ripple carry adder for a given set of inputs.

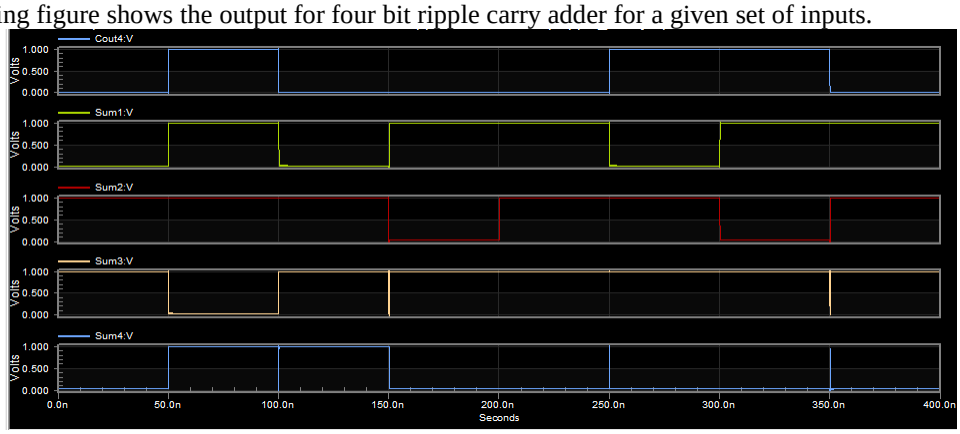


**Fig.12** Carry out and sum outputs for different set of inputs

In case of ripple carry adder, the transistor count is reduced to 88 transistors and the delay produced is 182.096ps. The average power consumed is 1.704641e-003 watts.

## VII. Design of carry look ahead adder using output wired cmos logic based majority gate

Carry look ahead adder is a kind of parallel adder. The adder uses the concept of propagation and generation of carry[15,18].The design of carry look ahead adder is based on following equation :

(i) Carry propagation : $P_i = A \oplus B$ (5)

(ii) Carry generation $G_i = A_i . B_i$ (6)

(iii) Sum $S_i = C_i \oplus P_i$ (7)

(iv) Carry out $C_{i+1} = G_i + P_i . C_i$ (8)

The adder is also called a fast adder because it adds two binary numbers and calculates carry bit before the sum is produced. It works on the principle of "generation and propagation of carry[21,22] bits". The carry propagator is propagated to the next level whereas the generator is used to generate the carry, regardless of its input. Carry look ahead adder [23]circuit diagram for one bit using logic gates is shown in Fig.13

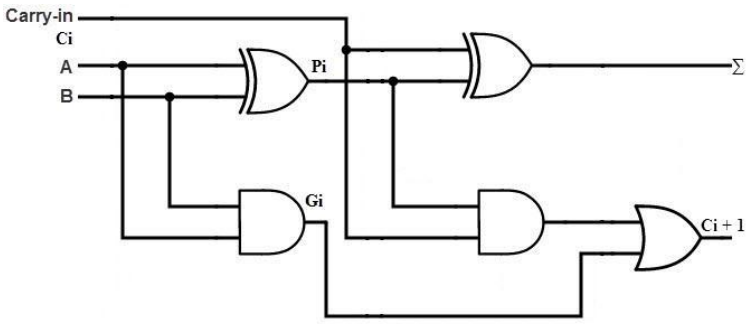


**Fig.13** Carry look ahead adder block diagram

For two bit, the block diagram can be shown as the following Fig.14 :

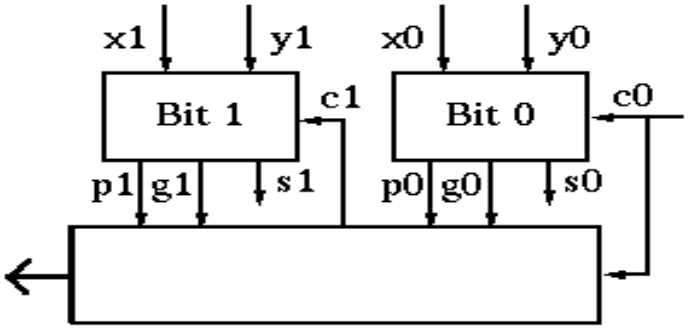


**Fig.14** 2 bit carry look ahead adder

The following Table shows the conditions where the carry will be generated or propagated.Here A,B and Ci are the inputs and Ci+1 is the carry for the next bit.

**Table 1** Carry generation and propagation based on input

| A | B | Ci | C i +1 | Condition |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | No carry generate |
| 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 0 | |
| 0 | 1 | 1 | 1 | No carry propagate |
| 1 | 0 | 0 | 0 | |
| 1 | 0 | 1 | 1 | |
| 1 | 1 | 0 | 1 | Carry generate |
| 1 | 1 | 1 | 1 | |

In the proposed design, Two bits are considered for each set of inputs. The inputs A1 and B1 are given as inputs along with C1 as the input carry and the second bit considered as input is A2 and B2. The bits are added and finally, the results are generated in the sum and carry output. The following Fig. shows the circuit design for the carry look ahead adder using majority gate.

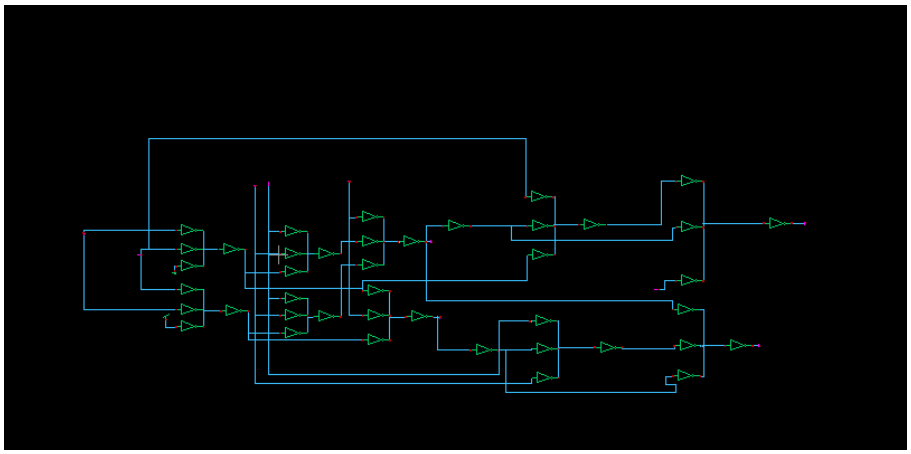

**Fig.15** Carry look ahead adder using output wired CMOS logic based majority gate

The results are produced where the outputs for carry and sum for each bit is calculated and produced in the output graph using Tanner tool. The simulation results for the above designed carry look ahead adder is as follows:

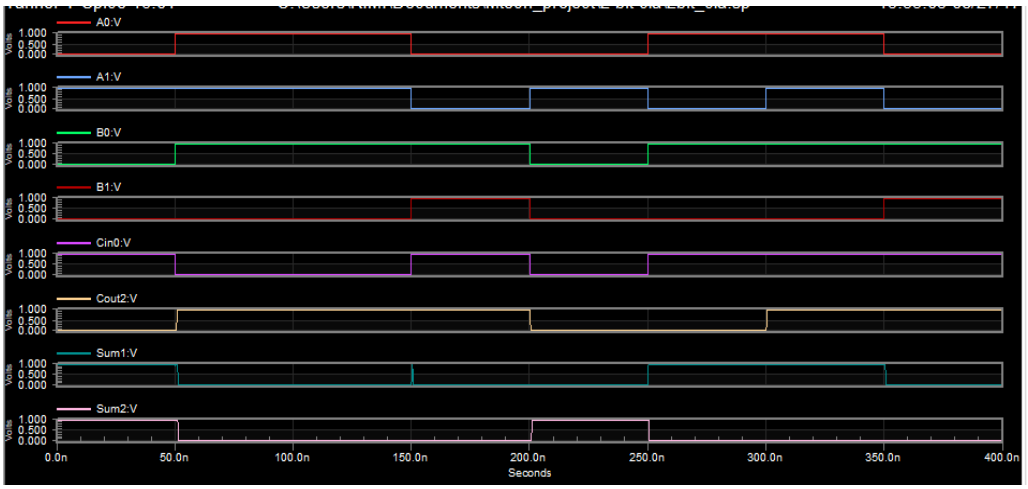


**Fig.16** Simulation result for carry look ahead adder

The simulation results show that the power consumed by the circuit design is 0.430703 * 10^(-3) watts and the delay calculated is -99.8060n while the transistor count is reduced to 84.

## VIII. Comparison Of Proposed Designs With Conventional Designs

A comparative study is being performed between the conventional and proposed designs for the different kinds of adder. The parameters considered for comparison are delay and transistor count. The following table shows the comparative results.

**Table 2**: Comparison between conventional and proposed design for following adders

| Design Name | Conventional Design | | Proposed Design | |
|---|---|---|---|---|
| | Delay | Transistor Count | Delay | Transistor Count |
| One bit full adder circuit | -199.5013n | 28 | -199.768ns | 22 |
| 4 bit ripple carry adder circuit | 55.63ns | 112 | 182.096ps | 88 |
| 2 bit carry look ahead circuit | 187.8ns | 98 | -99.8060ns | 84 |

## IX. Conclusion

The circuits have been designed using output wired CMOS logic based majority gate for 130 nm channel length. Two parameters important for design consideration are delay and area. In the proposed designs for three different kinds of adders, delay and transistor count is found to be less than the conventional design.

## Acknowledgement

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## References

**Proceedings Papers:**

[1]. *A Threshold Logic Full Adder Based on Resonant Tunnelling Transistors*, published at: ESSCIRC'98

[2]. R. Shalem, E. John, and L. K. John, *—A novel low-power energy recovery full adder cell,‖ in Proc. Great Lakes Symp. VLSI, Feb. 1999, pp. 380–383*

[3]. H. T. Bui, Y. Wang, and Y. Jiang, *"Design and Analysis of 10- Transistor Full Adders Using XOR-XNOR Gates," IEEE Trans. Circuits and Syst. II, Analog Digit. Signal Process., vol 49, no. 1, pp. 25-30, Jan. 2002.*

[4]. K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavei, *"A Novel Low Power Full-Adder Cell for Low Voltage," Integration the VLSI Journal, 2009*

[5]. S. Veeramachaneni, M. B. Sirinivas, *"New Improved 1-Bit Full Adder Cells",CCECE/CGEI, Canada, 2008*

[6]. P.K. Sinha Roy, *'' Test & realization of linearly separable switching functions'', Int. J. Control, 1970, Vol.11, No.5, 873-89*

[7]. T. Shibata and T. Ohmi, *—An intelligent MOS transistor featuring gate-level weighted sum and threshold operations,‖ in IEDM, Technical Digest, New York, NY, USA, Dec 1991, IEEE.*

[8]. H. O¨ zdemir, A. Kepkep, B. Pamir, Y. Leblebici, and U. C¸ iliniro˘glu, *—A capacitive threshold-logic gate,IEEE JSSC, vol. 31, no. 8, pp. 1141–1149, August 1996.*

[9]. P. Celinski, J. F. L´opez, S. Al-Sarawi, and D. Abbott, *—Low power, high speed, charge recycling CMOS threshold logic gate,IEE Electronics Letters, vol. 37, no. 17, pp. 1067–1069, August 2001.*

[10]. Mili Sarkar, Sunit Das, Upasana Roy Chowdhury, Dibyajyoti Das *— Design of Sequential Circuits using Single Electron Encoded Logic \IEMCON 2012.*

[11]. J. Fernandez Ramos, J. A. Hidalgo Lopez, M. J. Martin, J. C. Tejero, and A. Gago, *—A threshold logic gate based on clocked coupled inverters,International Journal of Electronics, vol. 84, no. 4, pp. 371–382, 2001*

[12]. Y Taur , D.A. Buchanan, W. Chen , D. Frank, K. Ismail, H. Wann,S. Wind, and H. Wong. *CMOS Scaling into the Nanometre Regime. Proceeding of the IEEE, Vol. 85(No.4):pp.486-504, 1997.*

[13]. IEEE Transactions On Neural Networks, vol. 14, no. 5, september 2003 *VLSI Implementations of Threshold Logic—A Comprehensive Survey.*

[14]. *Hazard-free edge-triggered D flipflop based on threshold gates*,J.M.Quintana ,M.J. Avedillo and A Rueda

[15]. Amelifard, Behnam, Farzan Fallah, and Massoud Pedram. *"Closing the gap between Carry Select Adder and Ripple Carry Adder: a new class of low-power high-performance adders." Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium on. IEEE, 2005.*

[16]. M Sarkar, SD Chowdhury, D Das, S Chowdhury, CD Choudhuri, M Basu *'DC analysis of a MOS based NDR circuit'published in IEEE Information Technology, Electronics and Mobile Communication Conference,2016*

[17]. M Sarkar, SN Ray, S Halder, D Das, R Sengupta *'Evolution of CMOS based NDR and its various applications'published in IEEE Information Technology, Electronics and Mobile Communication Conference .2016*

[18]. Kim, Youngjoon, and Lee-Sup Kim. *"A low power carry select adder with reduced area." Circuits and systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on. Vol. 4. IEEE, 2001.*

[19]. Sarkar, Mili, G. S. Taki, Rimi Sengupta, and Soham Nandi Ray. "*Design of ripple carry adder using CMOS output wired logic based majority gate." In Industrial Automation and Electromechanical Engineering Conference (IEMECON), 2017 8th Annual, pp. 328-331. IEEE, 2017.*

**Journal Papers:**

[20]. Devi, Padma, Ashima Girdher, and Balwinder Singh. *"Improved carry select adder with reduced area and low power consumption" International Journal of Computer Applications 3.4 (2010): 14-18.*

[21]. *Design and analysis of carry look ahead adder using CMOS technique* IOSR journal IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) e-*ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 9, Issue 2, Ver. VII (Mar - Apr. 2014), PP 92-95*

[22]. Celinski, Peter, et al. "S*ub-5.5 FO4 delay CMOS 64-bit domino/threshold logic adder design*." Microelectronics: *Design, Technology, and Packaging. Vol. 5274. 2004.*

[23]. Desoete, Bart, and Alexis De Vos. "*A reversible carry-look-ahead adder using control gates." Integration, the VLSI Journal 33.1 (2002): 89-104.*

[24]. Mili Sarkar, Shilpi Raj,Prasenjit Sengupta '*Design of Sequential circuits using Threshold Logic'UACEE International Journal of Advancements in Electronics and Electrical Engineering Volume 2: Issue 1 [ISSN: 2319 – 7498]*

[25]. Navi, Keivan, et al. *"Five-input majority gate, a new device for quantum-dot cellular automata." Journal of Computational and Theoretical Nanoscience7.8 (2010): 1546-1553*

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